## REMARKS

Claims 1-16 and 18-30 are canceled.

Claims 17 and 31-37 are pending.

Claims 17 and 31-37 are rejected.

The non-final office action dated July 10, 2009 indicates that base claim 31 remains rejected under 35 USC §102(e) as being anticipated by Ballagh U.S. Patent No. 6,883,147. The office action also indicates that base claim 35 remains rejected under 35 USC §103(a) as being unpatentable over Ballagh in view of admitted prior art. These rejections are respectfully traversed.

Consider a numerical simulation of a radar receiver processor. At the time the application was filed, the numerical simulation could take approximately two weeks of CPU time on a modern high-speed computer to provide 1.6 seconds of real-time radar data (page 2, lines 25-30 of the application)

Base claims 31 and 35 recite a method and system for improving the speed of a numerical simulation. The speed is improved by offloading a portion of the simulation from a computer to an FPGA, and managing the dataflow between the two.

The office action alleges that Ballagh discloses a method having all of the features recited in claim 31. It does not.

Base claim 31 recites

using a CPU to perform a numerical simulation including generating input signals and sending the input signals to an FPGA;

using the FPGA to apply a model to the input signals and send results of the model back to the CPU, the FPGA also generating a first output that marks data as valid or invalid, a second output that indicates the first sample of each frame, and a third output that indicates when the model can accept data; and

wherein the CPU uses the results in the numerical simulation and the outputs to maintain data flow with the FPGA.

Ballagh's Figure 2 illustrates a circuit design 200 including an FPGA 202 that communicates with an external processor. The functional requirements of the circuit design 200 are described at column 5, lines 4-38. That circuit design 200 does not perform a numerical simulation.

The office action says it does. It cites a paragraph starting at column 4, line 47. However, that paragraph does not describe the operation of the circuit design 200 of Figure 2. It describes the system of Figure 1.

Ballagh's Figure 1 illustrates a system for designing the FPGA 202 (col. 3, lines 63-65). An overview of the design process is described in Ballagh's Background section. The design process involves three phases: a specification phase, a modeling phase, and an implementation phase (col. 1, lines 17-22).

The specification phase involves defining functional requirements (col. 1, lines 19-20). The modeling phase involves capturing the design in executable form, simulating, and analyzing the results (col. 1, lines 31-32). The implementation phase involves creating a low-level hardware realization in terms of primitives in an appropriate technology library (col. 1, lines 47-58). Hardware languages such as VHDL are commonly used, as are libraries of intellectual property (IP) blocks.

Ballagh does not teach or suggest offloading a portion of the simulation from a computer to an FPGA. It follows that Ballagh is also silent about data flow between a computer running a portion of a numerical simulation and a FPGA running another portion of the numerical simulation.

The office action also alleges that data flow between the external processor and FPGA is described at column 5, line 28. It is not. That line and the preceding lines

describe a peripheral component 210, which is a finite impulse response (FIR) filter (col. 5, lines 19-20). A processor 204 controls filter reloading. As Ballagh says, the processor controls the filter reloading **from within the FPGA** (col. 5, lines 26-28).

Thus, Ballagh does not teach or suggest a method having all of the features recited in claim 31. Therefore, base claim 31 and its dependent claims 17 and 32-34 should be allowed over Ballagh.

Base claim 35 recites apparatus comprising a central processing unit (CPU) and a Field Programmable Gate Array (FPGA) for performing different portions of a numerical simulation.

> the CPU programmed to perform a numerical simulation of sine wave functions representing real and imaginary inputs;
>
> the FPGA programmed to perform a Fast Fourier Transform (FFT) on the inputs and send results of the FFT back to the CPU, the FPGA also generating a first output that marks data as valid or invalid, a second output that indicates the first sample of each frame, and a third output that indicates when the FFT can accept data;
>
> the CPU using the results in the numerical simulation and the outputs to maintain data flow with the FPGA.

As discussed above, Ballagh does not teach or suggest offloading a portion of a numerical simulation from a computer to an FPGA. Neither does the admitted prior art. The admitted prior art discloses the elements of a radar simulation. All elements are performed in a CPU. The admitted prior art also acknowledges a problem with the time needed to perform the simulation on a CPU (see page 2, lines 2-29 of the application). The claims recite an approach for speeding up the simulation. Ballagh does not teach or suggest the claimed approach. Therefore, base claim 35 and its dependent claims 36-37 should be allowed over Ballagh in view of the admitted prior art.

The Examiner is encouraged to contact the undersigned to resolve any remaining issues prior to mailing another office action.

Respectfully submitted,

/Hugh Gortler #33,890/
Hugh P. Gortler
Reg. No. 33,890
(949) 454-0898

Date: Oct. 13, 2009